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An Efficient Implementation Of Edge DetectionAlgorithm For Image Processing Using Fpga

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Abstract: Edge detection is an important and growing area indifferent fields such as image pattern recognition, machine learning and processing, and Computer vision. Edge detection of an image of the object is the main goal for different Edge detection algorithms. In Edge detection, the most important stepis to identify the edges of an image of the object and pixel information of the Image In every edge detection algorithm. There will be 2 types of masks one in the horizontal direction and the other in the vertical direction. The kernel or mask is a convolution vector of the nXn matrix which is multiplied by thesub-window of an image. The effective and efficient performance of a digital system mainly depends on the delay, area, and power consumption. These parameters decide the efficiency of any digital core system. This project converts the image pixel information to binary for processing with different edge detection algorithms like Canny, Sobel, Prewitt, and Roberts. The algorithms are then simulated and synthesized onFPGA with the targeted device xc3s4000-4fg900. The input image with resolution 256X256 is given as input to the MATLABversion 2014a. The MATLAB code converts image pixel intensity information to binary form as hardware input can onlybe in binary not the pixel intensity information, so we use MATLAB software to convert pixel intensity information to a hexadecimal value which is given as input to the model sim version 6.4a. The Different edge detection algorithm like Sobel, Canny, Prewitt, and Robert is implemented using Verilog HDL, the model sim is used for simulation, and synthesis is performedusing Xilinx software. The design parameters results obtained for different edge detection algorithms are compared, The Generated text file is sent to MATLAB software for the extraction of edges. and synthesis is performed in the Xilinx platform to generate a synthesis report for RTL schematic and Technology Schematic with a target device xc3s4000-4fg900. The Proposed methodology gives better performance with fewerlut's of 119, slices 77, gates 1736, overall delay 28.121ns, gate delay 15.304ns, and path delay 12.817ns along with 0 block ramand 0 distributed ram.

Keywords: FPGA, HDL, MATLAB, pixel, sub-window,recognition, Xilinx.

I. INTRODUCTION

Edge detection has many edge detection algorithms whichcan be used for image processing applications successfully. In edge detection methodology we determine the maximum or abrupt change in pixel intensity in an image, these changesin image pixel intensities are is indicated or identified by different edge detection algorithms, depending upon the salient features of an object the edges of an object are detected and also edge detection algorithms will remove the redundantparts from an image. After the edge detection mechanism, theoutput of these edge detector edges is classified into 2 types true edges and false edges, true edges are those which are correct and needed edges whereas false edges are unwanted or due to noise-formed edges and due to sensitiveness of a detector. An edge detection algorithm generally has 3 steps they are: filter, enhancement, and finally detection. first step Filtering is a process basically to eradicate the noise from the input image. The second step is for magnifying the image pixel intensity values in enhancement so that we can detect strong and meaningful edges. Nowadays as the technology is growing as well as the research on Artificial Intelligence computer visioning and in the mobile industry for figure print, pattern recognition in these fields of edge detection is becoming more important. Therefore, an effective edge detection algorithm is very important. There are different kinds of edge detection algorithms mainly Roberts, Prewitt, Sobel, and canny where it comes to performing speed, area and power consumption the Sobel edge detection algorithm has the upper hand as the computation complexity is less andis widely used in the more applications when its smooth and enhanced image canny has the upper hand but as its computational complexity is complex.

II. PROBLEM STATEMENT

The optimization of design parameters is the key requirement that is considered in designing a digital system. In the core image processing blocks, the major part is of the computational units basically multipliers, So the multiplier requirement leads to more area, power, and delay. As edge detection is based on basic matrix multiplication. Nowadays as improvement in the technology is gradually growing whereit needs to meet the performance requirement, in the applications like satellite monitoring, vehicle monitoring, and medical fields speed is important where in these places edge detection of an object is very important with faster response.

III. OBJECTIVE

1. To design an efficient modified Sobel edge detection algorithm using Verilog HDL for edge detection to reduce area, the computational complexity along with increased processing speed, and the reduced power consumption
2. To perform synthesis of the proposed Sobel edge detection along with canny, Roberts, and Prewitt edge detection algorithm and analyze the delay, area, and power consumption design parameters.
3. To implement the proposed Sobel edge detection algorithm in an image processing application. Like biomedical and satellite images, comparing the design parameters of Sobel, Canny, Prewitt, and Roberts.

IV. PROPOSED METHODOLOGY

A. Proposed Methodology Flow Diagram

The below diagram, as shown in figure 1 represents the flow of the proposed methodology. The description of each block is discussed below

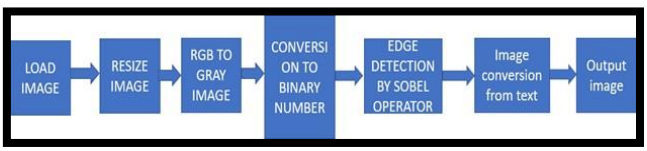


Figure 1:Methodology Flow Diagram

i. Load Image

The first step is to select the RGB image in JPG image format as an input image for the MATLAB code. The image(451x300) shown in figure 2(a) is selected as an input image in this proposed methodology

ii. Resize Image

the MATLAB code will convert the image for an equal resolution of 256X256 this is done by the resizing mechanism in MATLAB. The converted image from the resolution of 451x300 to 256x256 image is shown in figure 2(b).

iii. RGB To Gray Image

the resized image is then converted to the gray image as shown in figure 2(c), the MATLAB process. This conversionis done for reducing the memory size for processing the datain the model sim.

v. Edge Detection By Sobel Operator

For a Sobel Edge Detector, there are basically 2 types of masks or kernals, first is kernal which is shown in figure 4(a)gives us an edge in the horizontal direction when we convolve with the 3X3 sub-window of an image which is shown in figure 4(b). in the way, the second kernal in figure 4(a) givesthe edges in the horizontal direction when we convolved the second kernal with the 3X3 sub-window of an image.

-1	-2	-1		1	0	-1	D0	D1	D2
0	0	0		2	0	-2	D3	D4	D5
1	2	1		1	0	-1	D6	D7	D8

(a) **(b)**

Figure 4:(a) Sobel Operator Masks(b) Example 3X3 Subwindow of Image

Figure 5 shown below represents the convolution of thesource image sub-window with the kernal then we obtain a convolved image nothing but edge detected image.

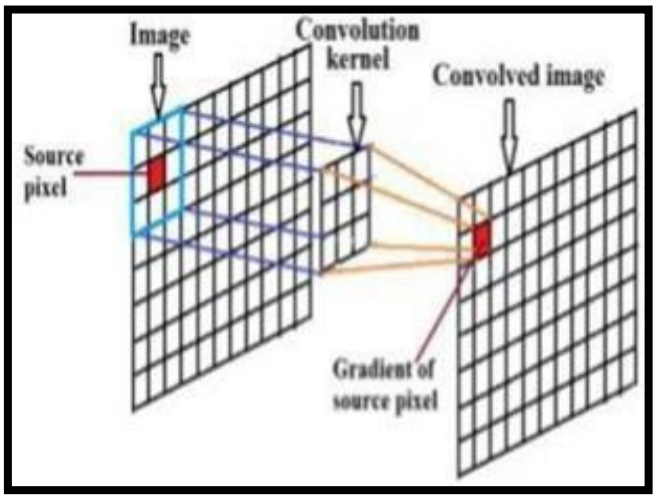
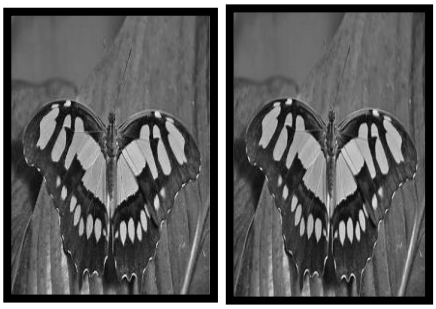


Figure 5:Edge Detection Using Sobel Operator

(a)



(b)

Figure 2:(a) Input image, (b)Resized Image, and (c)GrayImage

The flow diagram for the proposed architecture is representedin figure 6. The flow starts with aligning the input image andthen multiplying it with kernal using shift operator and adders. This image is further compressed from 9 source pixels (obtained after convolving 3x3 matrices) to 1-pixel information. The obtained pixel information is compared with the threshold voltage. If greater than the threshold value

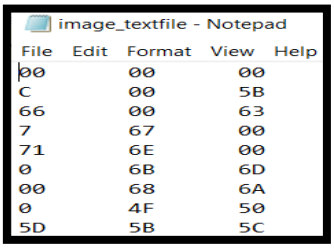
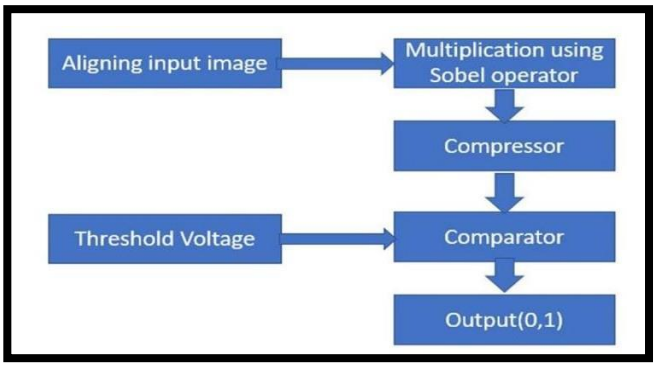


Figure 3: HexadecimalTexfile for an image



iv. Conversion To Binary Number

Then this gray pixel intensity information of an image is converted to binary form and stored in the text file as shown in figure 3. And this text file is given as input to the model sim platform, output is high else low.

Figure 6:Flow diagram for the Proposed architecture

The flow in figure 6, is explained in detail in figure 7. The clock reset and start are the global signals which are applied for all the blocks as we consider the 3X3 subblock of the image window as it consists of the 9 pixels with different intensity values all these signals are input and these pixels' information is given as input to the gy vertical gradient and gx horizontal gradient are calculated without any matrix multiplication instead we used the only adders and, shift operators so it leads to very minimum area efficient.

Then all these gy and gx is given as input for the gx_abs andgy_abs to get the absolute values i.e depending upon the msb bit gy and gx respectively for thegx_abs and gy_abs is its msb bit is 1 then gives an output of 2's complement else gives output the as same value.

Sum value is calculated on the summation of gx_abs and gy_abs then this output is transferred to the checkered part ofthe value is about the threshold, then the value of output dxywill be 1 i.e., respective central pixel else value of that respective pixel will be zero. This way with less computational complexity the working of the Sobel edge detector takes place with a better performance compared to the conventional approach.

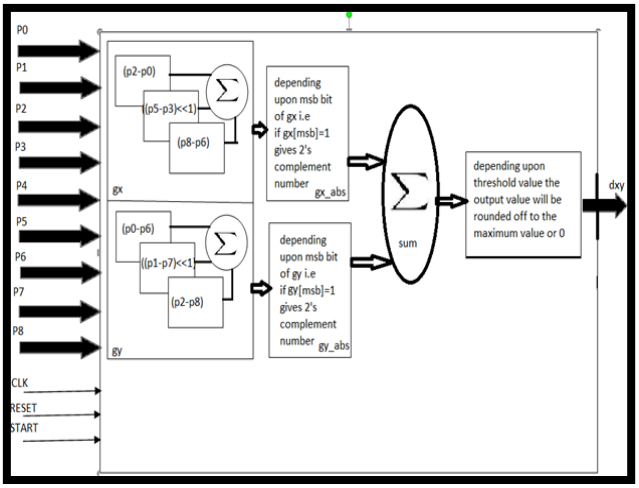


Figure 7:Proposed architecture

vi. Image Conversion from Text

After getting the output from the proposed architecture flowdiagram we get the following file where 0 represents low and255 represents high. This output is obtained from the model sim tool. These values are then fed to the MATLAB tool which processes this file to produce an edge detected as shown in figure 8.

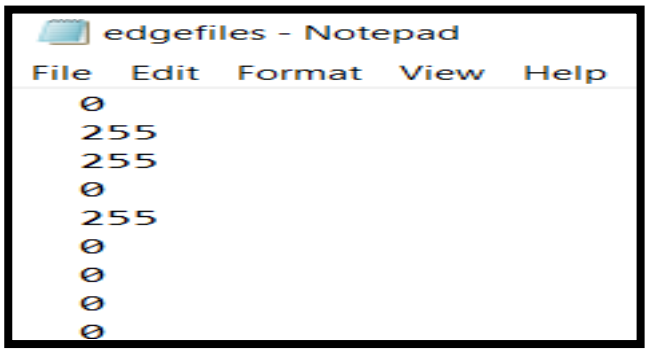


Figure 8:Edge Detected image TextFile

V. TOOLS USED

1. MATLAB
   a. To convert the RGB input image to a resizableimage
   b. To convert resizable image to gray image

c. This gray image consists of pixel intensity information this is converted to hexadecimal numbers and also vice versa.

2. Xilinx
   a. To get a synthesis report which consists area analysis report, power analysis report, and timing report
   b. To view the RTL schematic and as well as thetechnological schematic

3. Model Sim
   a. To briefly the functionality
   b. To view the waveforms

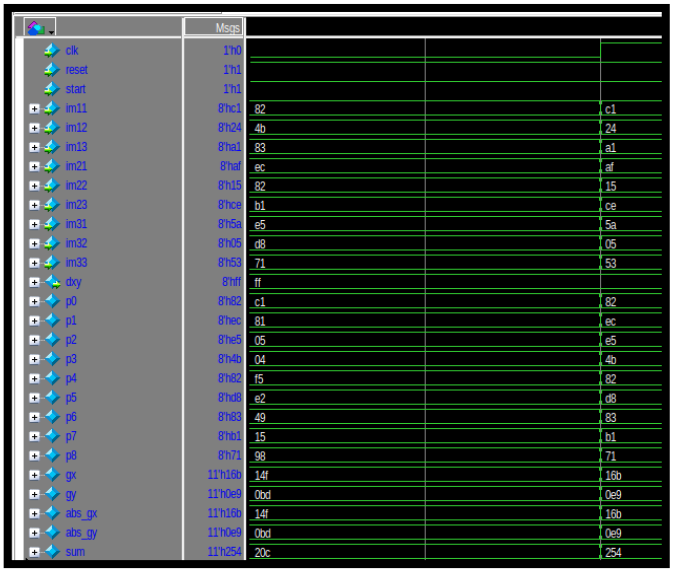


Figure 9:Sobel Edge Detector Simulation Result

The above figure shows a second instance of the Sobel edge detector with inputs c1, 24, a1, af, 15, ce, 5a, 05, and 53. On the clock signal set high, along with reset low and start signalhigh, the intermediate signals to calculate approximate expressions are initially get computed, and then finally, the approximate product is calculated. The approximate output isobserved to be 0 while the exact output equals some number below the threshold.

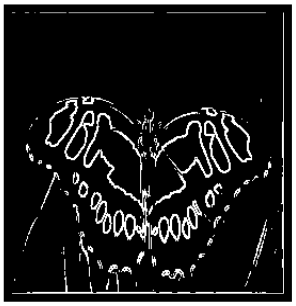
The output summary of constraint values in the designed Sobel, Canny, Prewitt, and Robert is as follows as shown in table 1. The comparison of synthesis results of the design constraint

VI. RESULTS

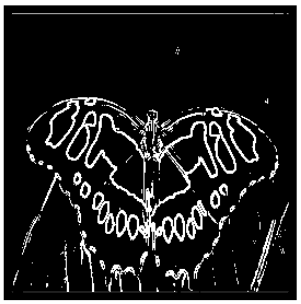
The simulations of the designed Sobel edge detector with the usage of appropriate adders and shift registers are obtained as observed in the following waveforms. The simulation outputs of the approximate Sobel edge detector areas follows as seen in the following snapshots in figure 9.

parameters such as delay, frequency, and slices in the Generic to the proposed Sobel edge detector is tabulated as seen in Tables 2 and 3. From the comparison and analysisof values in Tables 1, 2, and,3, the proposed Sobel edge detector with only an adder and shift register proves to be better performing both with regard to its processing speed and area consumption. The proposed Sobel edge detector delay was almost reduced to 1.2 times the delay of the Generic Sobel edge detector. The number of slices LUTs and their occupation in the proposed multiplier has also greatly decreased in the suggested approximate Sobel edge detector comparatively as observed in table 3.

Table 1:Comparision of Different Edge DetectionAlgorithms



(a)



(b)

Parameters	Sobel	Robert	Prewitt	Canny
Delay	28.121ns	33.229 ns	30.745 ns	33.115 ns
Frequency	35.6MHz	30.09MHz	32.52MHz	30.1MHz
LUTs	119	266	306	634

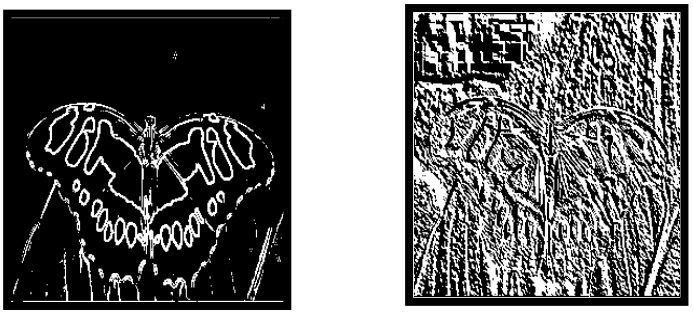
Table 2:Comparison of Delay for Generic and ProposedSobel Edge Detectors

Elements	Total Delay	Logical Delay	Routing Delay
Generic Sobel	31ns	18.5ns	12.5ns
Proposed Sobel	28ns	15ns	12 ns

Table 3:Comparison of Area for Generic and ProposedSobel Edge Detectors

Elements	No of Luts	No of slices	No of gates	No of IOBs
Generic Sobel	306	157	3761	182
Proposed Sobel	119	77	1736	75

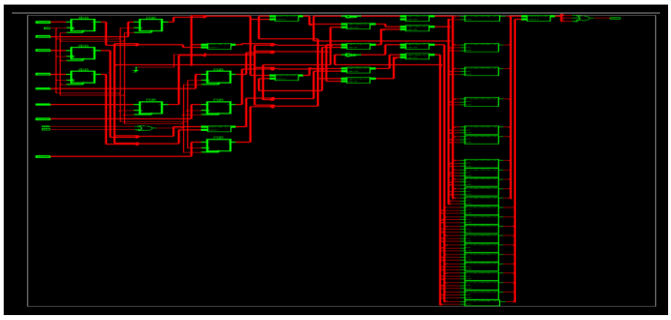
The figures in the proposed methodology-2(a), 2(b), and 2(c)shows 2(a) input image 2(b) resized images utilizing 2(c) gray image, and10(c) Sobel operator utilized only adders and shift operators where PSNR=8.42 for Sobel 10(b) PSNR=8.00 for canny 10(d) PSNR=5.21 for Robert 10(a) PSNR=8.3 for Prewitt and for Sobel with proposed approximate multiplier where PSNR=8.42. The input image and output edge detectedimages after applying the Sobel edge detection algorithm thatutilizes the accurate and the designed approximate Sobel operator in its operation are observed. With observation and analysis of the resultant output images, despite the fact that the approximate result is made use of, the designed Sobel edge detector, the difference cannot be recognized in the quality changes of the output image from the user level. Thereis the trivial quality of a change measured in terms of PSNR value. between the exact and all other edge detectors and the approximate Sobel edge detector image processing application. Hence, because of the restricted perceptiveness of the user in noticing quality difference variation in images, usage of approximation computations reducing computational complexity benefits speed and area.



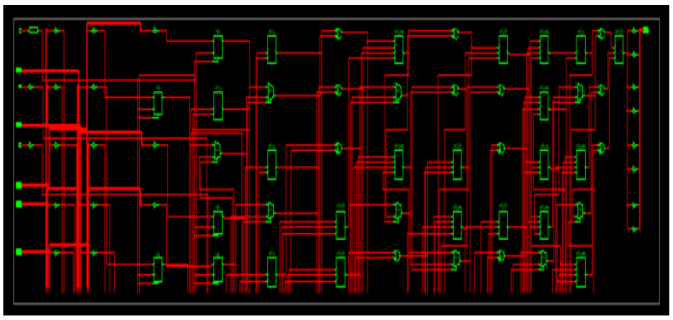
(c) (d)

Figure 10:(a) Prewitt Edge Image (b) Canny Edge Image(c)Sobel Edge Image and(d) Robert Edge Image

Figure 11(a)and11(b) is a RTL schematic and technological schematic view of the Sobel edge detector design where is a block view only signals can be viewed i.e. imp11, imp12, imp13, imp21, imp22, imp23, imp31, imp32, imp33 are the 8bit input for the block and clk, reset and start are one bit global signals these are provided from the user during testingwhere only one 8 bit output dxy. in the inner circuitry view all these are i.e. RTL is the image of the design independently of the FPGA circuit i.e. technology independent is RTL.



(a)



(b)

Figure 11: Schematic (a) RTL (b) Technological

VII. CONCLUSION

This project mainly focuses on the simulation of the designof the Sobel edge detection algorithm along with other edge detection algorithms for a better more realistic comparison. The proposed Sobel edge detection algorithm uses two kernalwhich is of 3×3 convolution masks to determine the edges along x and y direction and where in this project results are shown with reduced area power and latency for the Sobel edge detector and compared with all other edge detection Sobel proves to be more efficient and effective in terms

VIII. FUTURE SCOPE

- The Sobel edge detection proposed can also be extended to higher order image resolution where the performance of the Sobel edge detector is better, including the area and speed constraint parameters can show great improvement in comparison with the conventional Sobeledge detectors.
- The performance of the Sobel edge detector can further be improved by applying pulse width modulation, andtime-encoded signals.
- The usage of a more efficient adder and multiplier unit for obtaining better area utilization further can be considered to better the overall proficiency of the system.

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